IN THE SPECIFICATION:

Please amend paragraph number **[0002]** as follows:

[0002] Field of the Invention: This invention relates to integrated circuit manufacturing technology and, more specifically, to structures for making ~~low-resistance~~ low-resistance contact through a dielectric layer to a diffusion region in an underlying silicon layer. The structures include an amorphous titanium nitride barrier layer that is deposited via chemical vapor deposition.

Please amend paragraph number **[0006]** as follows:

[0006] Both reactive sputtering and nitrogen ambient annealing of deposited titanium result in films having poor step coverage, which are not useable in submicron processes. Chemical vapor deposition (CVD) processes have an important advantage in that conformal layers of any thickness may be deposited. This is especially advantageous in ~~ultra-large-scale-integration~~ ultra-large-scale integrated circuits, where minimum feature widths may be smaller than 0.5μm. Layers as thin as 10Å may be readily produced using CVD. However, TiN coatings prepared using the high-temperature atmospheric pressure CVD (APCVD) process must be prepared at temperatures between 900-1000° C. The high temperatures involved in this process are incompatible with conventional integrated circuit manufacturing processes. Hence, depositions using the APCVD process are restricted to refractory substrates such as tungsten carbide. The low-temperature APCVD, on the other hand, though performed within a temperature range of 100-400°C that is compatible with conventional integrated circuit manufacturing processes, is problematic because the precursor compounds (ammonia and $Ti(NR_2)_4$) react spontaneously in the gas phase. Consequently, special precursor delivery systems are required to keep the gases separated during delivery to the reaction chamber. In spite of special delivery systems, the highly spontaneous reaction makes full wafer coverage difficult to achieve. Even when achieved, the deposited films tend to lack uniform conformality, are generally characterized by poor step coverage, and tend to deposit on every surface within the reaction chamber, leading to particle problems.

Please amend paragraph number **[0012]** as follows:

[0012] Deposition of the titanium nitride barrier layer takes place in a low-pressure chamber ~~(i.e.~~ (i.e., a chamber in which pressure has been reduced to less than 100 torr prior to deposition), and utilizes a metal-organic tetrakis-dialkylamido-titanium compound as the sole precursor. Any noble gas, as well as nitrogen or hydrogen, or a mixture of two or more of the ~~foregoing~~ foregoing, may be used as a carrier for the precursor. The wafer is heated to a temperature within a range of 200-600° C. Precursor molecules which contact the heated wafer are pyrolyzed to form titanium nitride containing variable amounts of carbon impurities, which deposits as a highly conformal film on the wafer.

Please amend paragraph number **[0027]** as follows:

[0027] Although the compound deposited on the wafer with this process may be referred to as titanium carbonitride (represented by the chemical formula TiC_xN_y), the stoichiometry of the compound is variable, depending on the conditions under which it is deposited. The primary constituents of films deposited using the new process and tetrakis-dimethylamido-titanium as the precursor are titanium and nitrogen, with the ratio of nitrogen atoms to carbon atoms in the film falling within a range of 5:1 to 10:1. In addition, upon exposure to the atmosphere, the deposited films absorb oxygen. Thus the final film may be represented by the chemical formula $TiC_xN_yO_z$. The carbon and oxygen impurities affect the characteristics of the film in at least two ways. Firstly, the barrier function of the film is enhanced. Secondly, the carbon and oxygen impurities dramatically raise the resistivity of the film. Sputtered titanium nitride has a bulk sheet resistivity of approximately 75μohm-cm while the titanium carbonitride films deposited through the CVD process disclosed herein have bulk sheet resistivities of 2,000 to 50,000 μohm-cm. In spite of this dramatic increase in bulk resistivity, the utility of such films as barrier layers is largely unaffected, due to the characteristic thinness of barrier layers used in integrated circuit manufacture. A simple analysis of the contact geometry for calculating various contributions to the overall resistance suggests that metal (e.g.,

tungsten) plug resistance and metal-to-silicon interface resistance play a much more significant role in overall contact resistance than does the barrier layer.

Please amend paragraph number **[0030]** as follows:

[0030] The basic deposition process may be enhanced to further reduce the carbon content of the deposited titanium nitride film by introducing an activated species into the deposition chamber. The activated species attacks the alkyl-nitrogen bonds of the primary ~~precursor,~~ precursor and converts displaced alkyl groups into volatile compounds. The activated species, which may include halogen, NH_3, or hydrogen radicals, or a combination thereof, are generated in the absence of the primary precursor at a location remote from the deposition chamber. Remote generation of the activated species is required because it is not desirable to employ a plasma CVD process, as $Ti(NR_2)_4$ is known to break down in plasma, resulting in large amounts of carbon in the deposited film. A high carbon content will elevate the bulk resistivity of the film to levels that are unacceptable for most integrated circuit applications. The primary precursor molecules and the activated species are mixed, preferably, just prior to being ducted into the deposition chamber. It is hypothesized that as soon as the mixing has occurred, the activated species begin to tear away the alkyl groups from the primary precursor molecules. Relatively uncontaminated titanium nitride deposits on the heated wafer surface.

Please amend paragraph number **[0033]** as follows:

[0033] Referring now to FIG. 3, which is but a tiny cross-sectional area of a silicon wafer undergoing an integrated circuit fabrication process, a contact opening 31 having a narrow aspect ratio has been etched through a borophosphosilicate glass (BPSG) layer 32 to a diffusion region 33 in an underlying silicon substrate 34. A titanium metal layer 35 is then deposited over the surface of the wafer. Because titanium metal is normally deposited by sputtering, it deposits primarily on horizontal surfaces. Thus, the portions of the titanium metal layer 35 on the walls and at the bottom of the contact opening 31 are much thinner than the portion that is outside of the opening on horizontal surfaces. The portion of titanium metal layer 35 that covers diffusion

region 33 at the bottom of contact opening 31 will be denoted 35A. At least a portion of the titanium metal layer portion 35A will be converted to titanium silicide in order to provide a low-resistance interface at the surface of the diffusion region.

Please amend paragraph number **[0035]** as follows:

[0035] Referring now to FIG. 5, a high-temperature anneal step in an ambient gas such as nitrogen, argon, ammonia, or hydrogen is performed either after the deposition of the titanium metal layer 35 or after the deposition of the titanium nitride barrier layer 41. Rapid thermal processing (RTP) and furnace annealing are two viable options for this step. During the anneal step, the titanium metal layer portion 35A at the bottom of contact opening 31 is either partially or completely consumed by reaction with a portion of the upper surface of the diffusion region 33 to form a titanium silicide layer 51. The titanium silicide layer 51, which forms at the interface between the diffusion region 33 and titanium metal layer portion 35A, greatly lowers contact resistance in the contact region.